[0075] FIG. **6**D illustrates a fourth embodiment of a suitable protuberance **620**D. The protuberance has an approximately hemispherical shape. Notice that in contrast to the protuberances **220** of FIGS. **2**B-**2**C, the protuberance **620**D remains coupled with the semiconductor device **616** instead of with the substrate **612**. The approximately hemispherical shape of the protuberance faces the substrate instead of the semiconductor device. When the semiconductor device is separated from the substrate, the protuberance will remain coupled with the semiconductor device and will separate from the substrate. In some embodiments, the approximately hemispherically shaped protuberance may be operable to serve as a lens and/or focus light on the semiconductor device. By way of example, the semiconductor device may include a photovoltaic device and the lens shaped or light focusing protuberance may help to focus or concentrate solar radiation or other light onto the photovoltaic device. Alternatively, the semiconductor device may represent a photodiode array or other optical device. In other embodiments, rather than the approximately hemispherical shape, any other shape suitable to focus light and/or serve as a lens may be used instead. If the protuberance is formed of a graded composition release layer then the protuberance may represent a graded composition protuberance that has a graded composition across its thickness.

[0076] These are just a few representative examples of suitable sizes and shapes for protuberances **620** and/or non-flat surfaces. Those skilled in the art, and having the benefit of the present disclosure, will appreciate that various other sizes and shapes of protuberances and/or non-flat surfaces may be used instead. Various different shapes may be achieved depending upon the particular geometry and dimensions, the particular etch (e.g., the level of anisotropy), the particular grading, the particular effect of the grading on the etch rate, and the like. The particular grading (e.g., the compositions and the profiles of the compositions across the thickness of the graded composition release layer) may be modified to achieve a desired shape of a protuberance by those skilled, in the art and having the benefit of the present disclosure. For example, linear profiles, non-linear profiles, stepwise profiles, or combinations thereof may be selected for the gradation of the graded composition release layer in order to help tailor the shape. In addition, in some embodiments the composition of the graded composition release layer may also be modulated laterally in addition to being graded in the thickness of the layer. For example, material having a higher or lower composition of the salient component may be introduced at a central region between a semiconductor device and a substrate as compared to a periphery of the region between the semiconductor device and the substrate.

[0077] FIG. **7** is a block flow diagram of an embodiment of a method **704** of separating semiconductor devices from a substrate using first and second receiving substrates. The method includes coupling a first receiving substrate with a first portion or subset of the semiconductor devices formed over a substrate, at block **770**. In sonic embodiments, electrical contacts of the first receiving substrate and the first portion of the semiconductor devices may be physically and electrically coupled (e.g., using reflowed solder bumps). In some embodiments, a protuberance and/or non-flat surface may be disposed between each of the first portion of the semiconductor devices and the substrate. The first portion of the semiconductor devices may be coupled with the substrate by the protuberances and/or by anchors. The first receiving substrate and the first portion of the semiconductor devices may be separated from the substrate, at block **771**. A second receiving substrate may be coupled with a second, different portion or subset of the semiconductor devices formed over the substrate, at block **772**. In some embodiments, electrical contacts of the second receiving substrate and the second portion of the semiconductor devices may be physically and electrically coupled (e.g., using reflowed solder bumps). In some embodiments, a protuberance and/or non-flat surface may be disposed between each of the second portion of the semiconductor devices and the substrate. The second portion of the semiconductor devices may be coupled with the substrate by the protuberances and/or by anchors. The second receiving substrate and the second portion of the semiconductor devices may be separated from the substrate, at block **773**. In other embodiments, three or more different receiving substrates may optionally be used.

[0078] FIG. **8** is a block flow diagram of an embodiment of a method **880** of reusing a substrate. The method optionally includes separating semiconductor devices from a substrate, at block **881**. This may be done substantially as described in conjunction with FIG. **2**C and/or FIG. **3**I. In some embodiments, the substrate has protuberances coupled therewith between corresponding semiconductor devices and the substrate. The various protuberances disclosed elsewhere herein are suitable including their features and optional details. The method includes removing the protuberances from the substrate, at block **882**. In some embodiments, this may include etching the protuberances from the substrate. In other embodiments, this may include performing a chemical mechanical polishing (CMP) or other planarization operation. In still other embodiments, other surface planarization or material removal methods may optionally be used. In addition to the protuberances, such operations may also remove other structures or materials, such as, for example, the fixed structures **342**L, **342**R, other structures or materials over or at the same level as the protuberances, etc. The method optionally includes forming one or more semiconductor layers over the substrate after the removal of the protuberances, at block **883**. For example, this may be used to replace or increase the thickness of the group III-V compound semiconductor layer **312** if it has been removed or partially removed. In some embodiments, one or more layers may be epitaxially grown over the substrate. The method includes forming a layer, for example a graded composition release layer, over the substrate, at block **884**. The various graded composition release layers disclosed elsewhere herein are suitable including their features and optional details. Subsequently, other layers may be formed, such as, for example, group III-V compound semiconductor device layers, and then the layers may be processed substantially as described elsewhere herein to release and separate semiconductor devices. In other cases, other layers besides a graded composition release layer may be formed over the substrate. For example, this may be the case when the substrate is reused to form other types of devices that utilize different types of layers. Advantageously, the ability to reuse the substrate may help to reduce manufacturing costs.

[0079] In the description above, embodiments have been shown and described as using a graded composition release layer. As described, the grading of the composition of the graded composition release layer may change the etch rate of the etch used to etch the layer and may be used as a way to help control the shape and size of the protuberances. Often such grading may allow more control over the shape. How-